ABSTRACT

The invention provides a directional ion etching process to pattern self-aligned via contacts in the manufacture of semiconductor devices such as high density magnetic random access memory (MRAM). In a particular embodiment, a semiconductor wafer is prepared with vertically arranged layers, including a patterned layer in electrical contact with a conductive row layer. The patterned layer may be a magnetic tunnel junction layer. A photoresist is deposited on the junction layer, masked, exposed and developed. The non-protected junction layer is etched to provide appropriate junction stacks. The remaining photoresist caps are not dissolved, rather they and the surface of the wafer are coated with a dielectric. Directional ion etching at a low angle relative to the junction stack layer removes the coated photoresist caps and thereby provides at least one patterned self-aligned via contact.